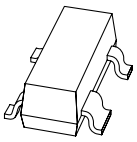

PRTR5V0U2X

Ultra low capacitance double rail-to-rail ESD protection diode

Rev. 02 — 14 January 2008 Product data sheet

1. Product profile

1.1 General description

Ultra low capacitance rail-to-rail ElectroStatic Discharge (ESD) protection diode in a small SOT143B Surface-Mounted Device (SMD) plastic package designed to protect two Hi-Speed data lines or high-frequency signal lines from the damage caused by ESD and other transients.

PRTR5V0U2X incorporates two pairs of ultra low capacitance rail-to-rail diodes as well as an additional ESD protection diode to ensure signal line protection even if no supply voltage is available.

1.2 Features

- ESD protection of two Hi-Speed data lines or high-frequency signal lines
- Ultra low input/output to ground capacitance: $C_{(I/O-GND)}$ = 1 pF
- ESD protection up to 8 kV
- IEC 61000-4-2, level 4 (ESD)
- Very low clamping voltage due to an integrated additional ESD protection diode
- Very low reverse current
- Small SMD plastic package

1.3 Applications

- USB 2.0 ports
- Digital Video Interface (DVI) / High Definition Multimedia Interface (HDMI) interfaces
- Mobile and cordless phones
- Personal Digital Assistants (PDA)
- Digital cameras
- Wide Area Network (WAN) / Local Area Network (LAN) systems
- PCs, notebooks, printers and other PC peripherals

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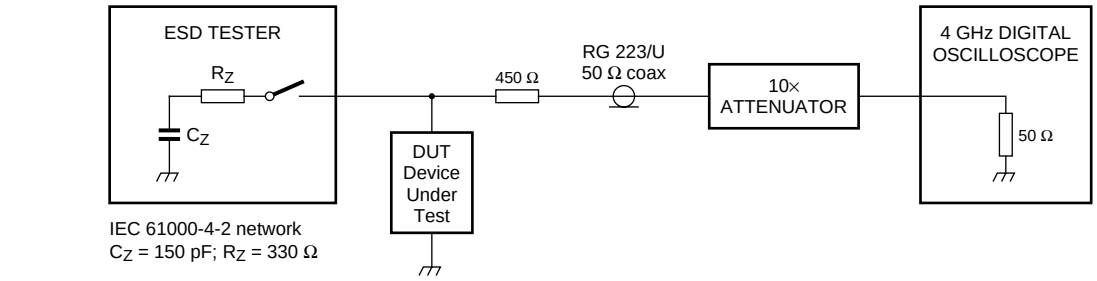
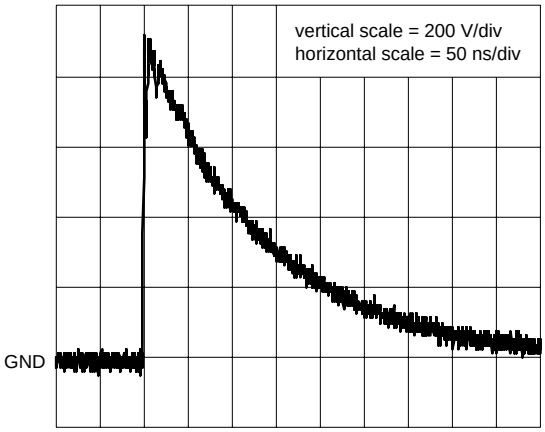
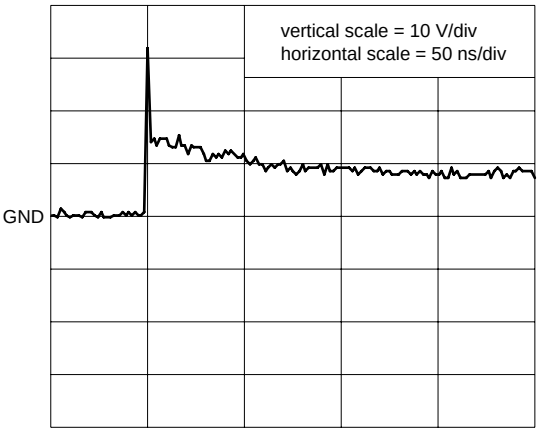


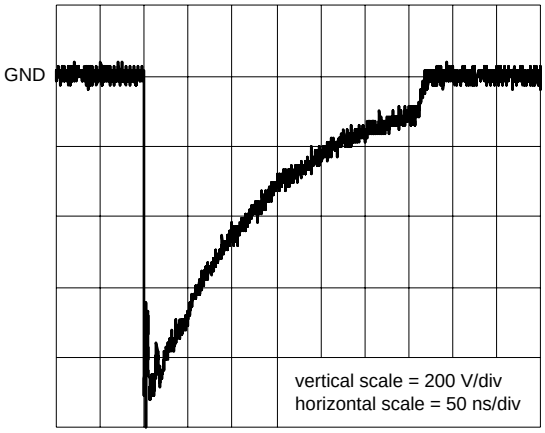
IEC 61000-4-2 network
C_Z = 150 pF; R_Z = 330 Ω



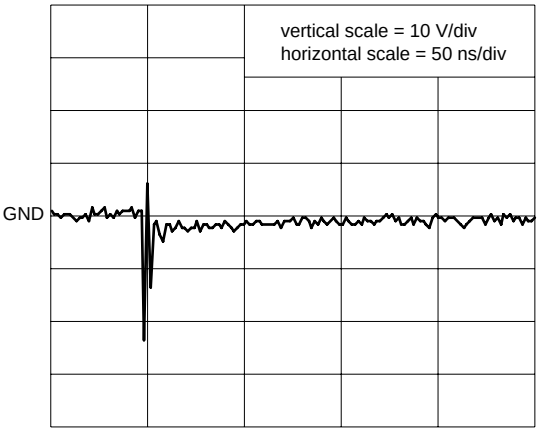
unclamped +1 kV ESD voltage waveform
(IEC 61000-4-2 network)



clamped +1 kV ESD voltage waveform
(IEC 61000-4-2 network)



unclamped −1 kV ESD voltage waveform
(IEC 61000-4-2 network)



clamped −1 kV ESD voltage waveform
(IEC 61000-4-2 network)

006aab112

Fig 4. ESD clamping test setup and waveforms

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7. Application information

Handling data rates up to 480 Mbit/s, USB 2.0 interfaces require ESD protection devices with an extremely low line capacitance in order to avoid signal distortion.

With a capacitance of only 1 pF, the PRTR5V0U2X offers IEC 61000-4-2, level 4 compliant ESD protection.

The PRTR5V0U2X integrates two pairs of ultra low capacitance rail-to-rail ESD protection diodes and an additional ESD protection diode.

The additional ESD protection diode connected between ground and V_{CC} prevents charging of the supply.

To achieve the maximum ESD protection level, no additional external capacitors are required.

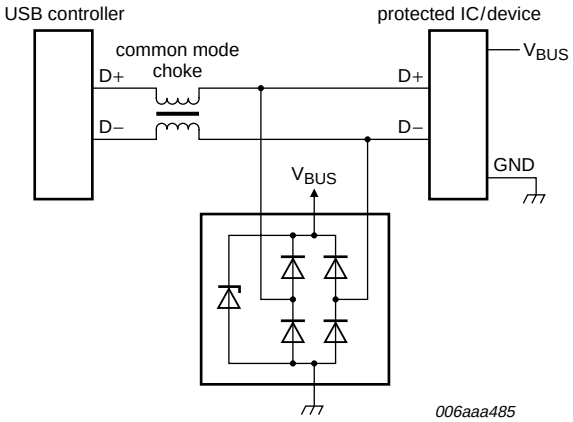

Fig 5. Application diagram: USB 2.0

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the PRTR5V0U2X as close to the input terminal or connector as possible.
2. The path length between the PRTR5V0U2X and the protected line should be minimized.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

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8. Package outline

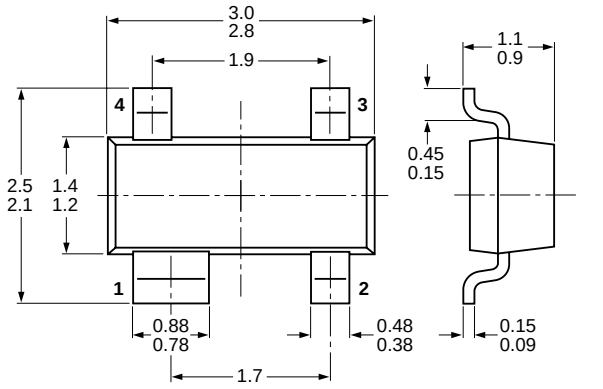

Fig 6. Package outline SOT143B

9. Packing information

Table 8. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.[1]

Type number	Package	Description	Packing quantity	
			3000	10000
PRTR5V0U2X	SOT143B	4 mm pitch, 8 mm tape and reel	-215	-235

[1] For further information and the availability of packing methods, see Section 13.

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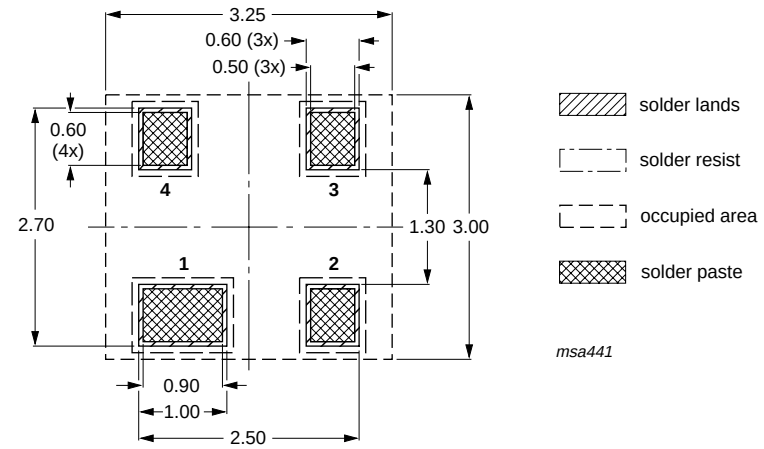
10. Soldering



Dimensions in mm

Fig 7. Reflow soldering footprint SOT143B

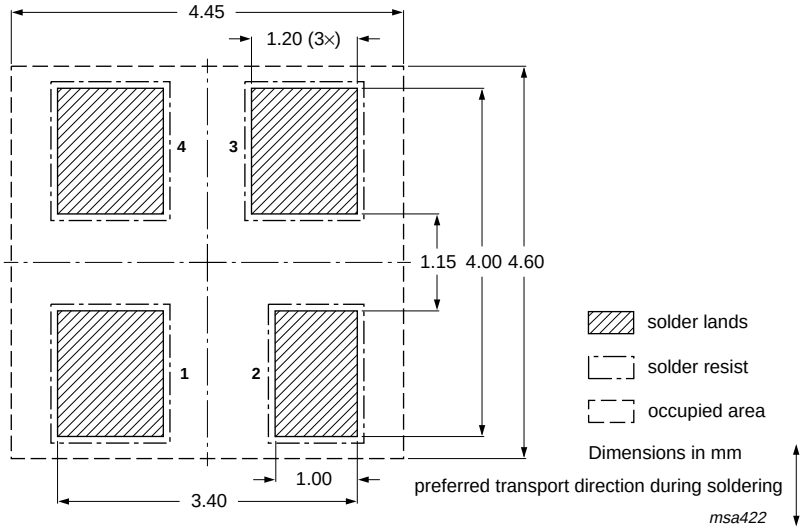


Fig 8. Wave soldering footprint SOT143B

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11. Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PRTR5V0U2X_2	20080114	Product data sheet	-	PRTR5V0U2X_1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Table 1: parameter for $C_{(I/O-GND)}$ redefined to input/output to ground capacitance • Table 1 “Quick reference data”: maximum value for $C_{(I/O-GND)}$ added • Table 7: parameter for $C_{(I/O-GND)}$ redefined to input/output to ground capacitance • Table 7 “Characteristics”: maximum value for $C_{(I/O-GND)}$ added • Table 7: parameter for $C_{(I/O-I/O)}$ redefined to input/output to input/output capacitance • Table 7: parameter for C_{sup} redefined to supply pin to ground capacitance • Section 10 “Soldering”: added • Section 12 “Legal information”: updated			
PRTR5V0U2X_1	20050922	Product data sheet	-	-

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12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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